

Short Papers

Design and Performance of GaAs DCFL Frequency Divider

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Abstract—GaAs frequency dividers for application to gigahertz-band equipment have been developed with E/D DCFL circuits. The relationship between maximum counting frequency and threshold voltage combination of the E-MESFET's and the D-MESFET's has been investigated in detail. The measured performance was as follows: maximum counting frequency is 1.1 GHz with low dissipation power of 17 mW, and the values of dissipation-power-divided-by-maximum-counting-frequency are as small as 1.6–16 pJ.

I. INTRODUCTION

GaAs MESFET logic, such as BFL, SDFL, or DCFL, have come to be used actively in recent years [1]. In the GaAs digital IC's previously reported, the BFL and SDFL configurations were widely used. These have the advantage of a wide logic swing when compared with the DCFL configuration. With respect to power dissipation and circuit simplicity, however, the DCFL configuration has capability for large-scale integration, while a strict circuit-design and fabrication-technology about threshold voltage optimization are required because threshold voltage limits logic speed.

In this work, GaAs E/D DCFL frequency dividers have been developed, and the relationship between maximum counting frequency and threshold voltage combination of the E-MESFET's and the D-MESFET's has been shown in detail.

II. CIRCUIT DESIGN AND FABRICATION

GaAs E/D DCFL frequency dividers with 5- μm , 10- μm , and 20- μm gate widths were constructed. A photograph of the divider chip (20- μm gate width) is shown in Fig. 1. The divider consists of a master/slave flip-flop and an output buffer circuit. Gate length is 1.2 μm . Both inter-gate-source length and inter-gate-drain length are as short as 0.4 μm [2]. From the computer-aided divider circuit simulation using a GaAs MESFET equivalent circuit [3], [4], the threshold voltages of the E-MESFET's and the D-MESFET's were chosen as follows: $V_{thE} = -0.1$ – $+0.27$ V and $V_{thD} = -0.67$ – -0.25 V.

The active layers for the E-MESFET's and the D-MESFET's were fabricated by ion-implantation technique [5]. The Schottky-barrier gates and ohmic contacts were fabricated using Al and AuGe–Ni evaporation, respectively.

III. PERFORMANCE

The relation between maximum counting frequency and threshold voltage combination of the E-MESFET's and the D-MESFET's was investigated in detail. As shown in Fig. 2, the

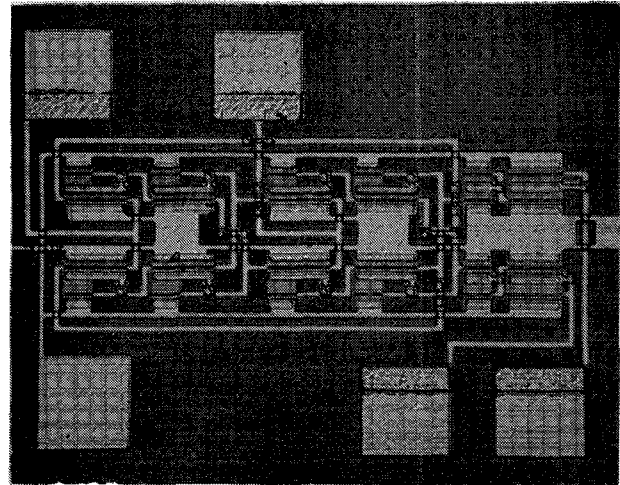


Fig. 1. Photograph of the GaAs divider chip.

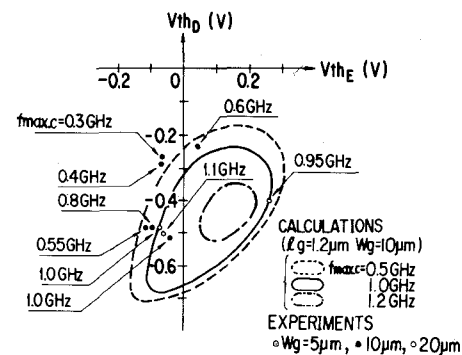


Fig. 2. Maximum counting frequency versus threshold voltage of the E-MESFET's as switching elements and the D-MESFET's as load elements.

measured relations obtained for a lot of dividers agreed well with the calculated result which was obtained from the divider circuit simulation using a GaAs MESFET equivalent circuit [3], [4]. The optimum values of V_{thE} and V_{thD} for the highest speed operation lie around 0.1 V and -0.4 V, respectively.

The relationship between measured values of maximum counting frequency and dissipation power was found as shown in Fig. 3. Compared with GaAs binary frequency dividers previously reported [6]–[10], the dividers developed in this work can operate with relatively low dissipation power (less than 17 mW including the power at the output buffer circuit), while retaining the high-speed operation (up to 1.1 GHz). The small values of 1.6–16-pJ dissipation-power-divided-by-maximum-counting-frequency (P_{dis}/f_{max-c}), which corresponds to the requisite minimum energy for divider operation, are attained with the dividers developed in this work, while the values are from 6 pJ to 100 pJ with the GaAs dividers previously reported. The low-power operation of the present dividers discussed above shows that the divider-circuit construction adopted in this work would be useful to larger scale integration (e.g., a prescaler IC's fabrication).

Fig. 4 shows input/output waveforms for the divider (20- μm

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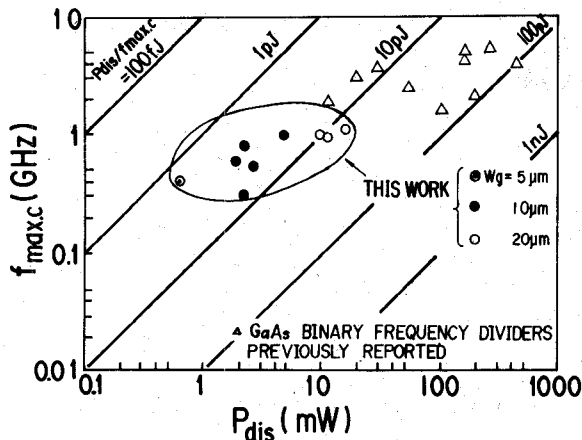


Fig. 3. Relationship between dissipation power and maximum counting frequency.

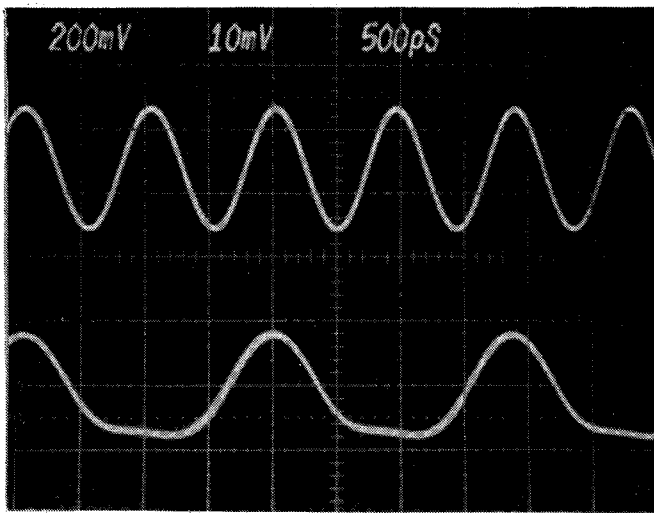


Fig. 4. Input/output waveforms of the developed divider.

gate width) at 1.1-GHz input frequency, which were observed by a 50- Ω system connected to the drain of the output buffer circuit.

IV. CONCLUSION

GaAs frequency dividers for application to gigahertz-band equipment have been developed with E/D DCFL circuits. The relationship between maximum counting frequency and threshold voltage, which are the critical design parameters of the divider circuit, have been shown in detail. The measured performance was as follows: maximum counting frequency is 1.1 GHz with low dissipation power of 17 mW, and the values of dissipation-power-divided-by-maximum-counting-frequency are as small as 1.6–16 pJ.

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Losses in Coplanar Waveguides

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Abstract—Conductor losses in coplanar waveguides have been calculated using a quasi-static Green's function approach. These calculations and others on dielectric and radiation losses are used to compute the quality factor of half-wavelength resonators, and comparison with measurements show good agreement.

I. INTRODUCTION

The coplanar waveguide (CPW) is a planar guiding structure (Fig. 1) sometimes suggested as an alternative to microstrip lines [1], [2] in both hybrid and monolithic circuits. Losses in these guides have been investigated by several authors [3]–[6] over a limited range of parameters.

The present paper calculates the conductor losses in a coplanar waveguide, using a quasi-static approach, and provides a comprehensive set of results. The quality factors of half-wavelength resonators including radiation losses are calculated and the results are compared with experimental measurements on resonators on substrates with a relative dielectric constant ϵ_r of 13.0.

II. CALCULATION OF COPLANAR WAVEGUIDE PARAMETERS

The various parameters of the coplanar waveguide are calculated for different strip width to ground plane spacing ratios ($2a/2b$) (see Fig. 1), assuming quasi-static TEM propagation.

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